	Time Stamp	Comment	Error Definition	Er ro
1	2003/08/2 0 16:20			0
2	2003/08/2 0 16:10			0
3	2003/08/2 0 16:11			0
4	2003/08/2 0 16:18			0
5	2003/08/2 0 16:21			Ο
6	2003/08/2 0 16:21			Ο
7	2003/08/2 0 16:21			0

	Туре	L #	Hits	Search Text	DBs
1	BRS	L1	652	(block near5 (error near4 rate))	USPA T
2	BRS	L2	78	1 and (optic\$4 near4 (dis\$1 record))	USPA T
3	BRS	L4	48	2 and (averag\$5)	USPA T
4	BRS	L3	3	2 and (count\$5 same reset\$5)	USPA T

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	Time Stamp	Comment	Error Definition	Er ro rs
1	2003/08/2 0 16:10			0
2	2003/08/2 0 16:10		***************************************	0
3	2003/08/2 0 16:11			0
4	2003/08/2 0 16:18		***************************************	0

	Туре	L #	Hits	Search Text	DBs
1	BRS	L1	21310	error near4 rate	USPA T
2	BRS	L2	298	1 same sector	USPA T
3	BRS	L3	30	2 same averag\$5	USPA T
4	BRS	L4	19764	error near4 rate	US-P GPUB; EPO; JPO; DERW ENT; IBM_ TDB
5	BRS	L5	178	4 same sector	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB
6	BRS	L6	9	5 same averag\$5	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB
7	BRS	L7	3678	(("c1" "c2")same error)	USPA T
8	BRS	L8	629	7 and (count\$5 same reset\$5)	USPA T
9	BRS	L9	238	8 and averag\$5	USPA T
10	BRS	L10	38	9 and (optic\$4 near4 (dis\$1 record))	USPA T
11	BRS	L11	1802	1 same averag\$5	USPA T
12	BRS	L12	119	11 and (optic\$4 near4 (dis\$1 record))	USPA T
13	BRS	L13	41	12 and (count\$5 same error)	USPA T
14	BRS	L14	41	12 and (count\$5 same error)	USPA T

	Time Stamp	Comment	Error Definition	ro
1	2003/08/2 1 07:12			0
2	2003/08/2 1 07:04			0
3	2003/08/2 1 07:30			0
4	2003/08/2 1 07:12			••••••••••••••••••••••••••••••••••••••
5	2003/08/2 1 07:12			О
6	2003/08/2			Ο
7	2003/08/2 1 07:17			0
8	2003/08/2			0
9	2003/08/2			0
10	2003/08/2			0
11	2003/08/2		***************************************	0
12	1 07:30 2003/08/2		***************************************	n
13	1 07:37 2003/08/2		**************************************	0
	1 07:37 2003/08/2 1 07:37			

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	Туре	L #	Hits	Search Text	DBs
1	BRS	L1	24898	error near4 rate	USPA T
2	BRS	L2	2097	1 same averag\$5	USPA T
3	BRS	L3	335	2 and (count\$5 same reset\$5)	USPA T
4	BRS	L4	47	3 and (register same threshold)	USPA T
5	BRS	L5	47	4 and (compar\$5)	USPA T
6	BRS	L6	21588	error near4 rate	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB
7	BRS	L7	1040	6 same averag\$5	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB
8	BRS	L8	81	7 and (count\$5 same reset\$5)	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB
9	BRS	L9	67	8 and compar\$5	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB

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	Time Stamp	Comment s	Error Definition	Er ro rs
1	2003/08/2 1 08:11			0
2	2003/08/2 1 08:08			0
3	2003/08/2 1 08:08			0
4	2003/08/2 1 08:09			0
5	2003/08/2 1 08:09			0
6	2003/08/2 1 08:11			Ο
7	2003/08/2 1 08:11			Ο
8	2003/08/2 1 08:12			Ο
9	2003/08/2 1 08:16			0

	Туре	L #	Hits	Search Text	DBs
10	BRS	L10	O	and (threshold near5 register)	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB
11	BRS	L11	1	and (threshold near5 register)	US-P GPUB ; EPO; JPO; DERW ENT; IBM_ TDB

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	Time Stamp	Comment	Error Definition	Er ro rs
10	2003/08/2 1 08:16			О
11	2003/08/2 1 08:16			Ο

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SEE OR SEARCH CLASS:

360, Dynamic Magnetic Information Storage or Retrieval, 26 for electronically correcting phasing errors between related information signals.

Data formatting to improve error detection correction capability:

This subclass is indented under the class definition. Subject matter in which a change in data format or sequence is utilized to improve the error detection/correction capability of a coding scheme.

Memory access (e.g., address permutation):

This subclass is indented under subclass 701. Subject matter which changes the format of digital data by having the signal with the data written into or read out of a storage device.

(1) Note. Address permutation arrangements are included in this subclass.

SEE OR SEARCH THIS CLASS, SUBCLASS:

718, for diagnostic testing of a memory.

703 Testing of error-check system:

This subclass is indented under the class definition. ISubject matter in which the proper operation of the error detection/correction or fault detection/recovery apparatus itself is verified.

704 Error count or rate:

This subclass is indented under the class definition. Subject matter which determines the number of bits in error or the number of bits in error per unit of time.

SEE OR SEARCH THIS CLASS, SUBCLASS:

798, for this subject matter combined with control of synchronization in response to an error detection signal.

705 **Pseudo-error rate**:

This subclass is indented under subclass 704. Subject matter having a main data path and a secondary data path having intentionally degraded performance connected in parallel, the secondary path having a decision device to compare and evaluate the disagreement between the paths.

(1) Note. Each disagreement is called a pseudo-error.

706 **Up-down counter:**

This subclass is indented under subclass 704. Subject matter including an reversible accumulating register which counts up in response to an error and counts down in response to an error-free increment of time.

SEE OR SEARCH CLASS:

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, appropriate subclasses for up-down counters per se.

Synchronization control:

This subclass is indented under subclass 704. Subject matter in which a determination of the error rate is used to control synchronization between devices.

SEE OR SEARCH THIS CLASS, SUBCLASS:

798+, for error detection controlled synchronization control other than by error rate.

Shutdown or establishing system parameter (e.g., transmission rate):

This subclass is indented under subclass 704. Subject matter including control of system operation by either deactivation of the system, or controls a parameter related to normal system operation, in response to error count or error rate.

709 Data pulse evaluation/bit decision:

This subclass is indented under subclass 699. Subject matter in which the information bearing parameter (amplitude, pulse position, etc.) of a data pulse is evaluated to determine the proper logic state or value.

(1) Note. Subject matter in this subclass relates to determining if a data pulse represents a particular given logic state, e.g., logic one as opposed to logic zero.

SEE OR SEARCH CLASS:

- 327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, 1+ for pulse selecting means.
- 329, Demodulators, 311+ for pulse demodulation or detection, per se.

Replacement of memory spare location, portion, or segment:

This subclass is indented under subclass 699. Subject matter in which the spare apparatus comprises only a location, or a contiguous group of locations of memory.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, 200 and 201 for bad bit and testing read /write circuits, respectively.

Spare row or column:

This subclass is indented under subclass 710. Subject matter spare apparatus comprises only a column or row within a memory device or element.

712 Transmission facility testing:

This subclass is indented under subclass 699. Subject matter in which the diagnostic testing is performed upon a channel of a transmission medium with a device for supplying digital data thereto.

(1) Note. The transmission facility includes the transmission medium and all associated equipment required to transmit a message.

SEE OR SEARCH CLASS:

- 370, Multiplex Communications, 241+ for testing of multiplex communication systems.
- 375, Pulse or Digital Communications, 224+ for testing of pulse or digital communications system.
- 379, Telephonic Communications, 1.01-33 for diagnostic testing of telephone equipment.

713 For channel having repeater:

This subclass is indented under subclass 712. Subject matter wherein a transmission channel has a repeating amplifier.

714 **By tone signal**:

This subclass is indented under subclass 712. Subject matter which includes application of a test signal composed of one or more tone signals.

	Туре	L #	Hits	Search Text	DBs
1	BRS	L1	652	(block near5 (error near4 rate))	USPA T
2	BRS	L2	78	l and (optic\$4 near4 (dis\$1 record))	USPA T
3	BRS	L4	48	2 and (averag\$5)	USPA T
4	BRS	L3	3	2 and (count\$5 same reset\$5)	USPA T
5	BRS	L5	511	(block near5 (error near4 rate))	US-P GPUB; EPO; JPO; DERW ENT; IBM_ TDB
6	BRS	L6	172	5 and (averag\$5)	US-P GPUB; EPO; JPO; DERW ENT; IBM_ TDB
7	BRS	L7	15	6 and (count\$5 same reset\$5)	US-P GPUB; EPO; JPO; DERW ENT; IBM_ TDB

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